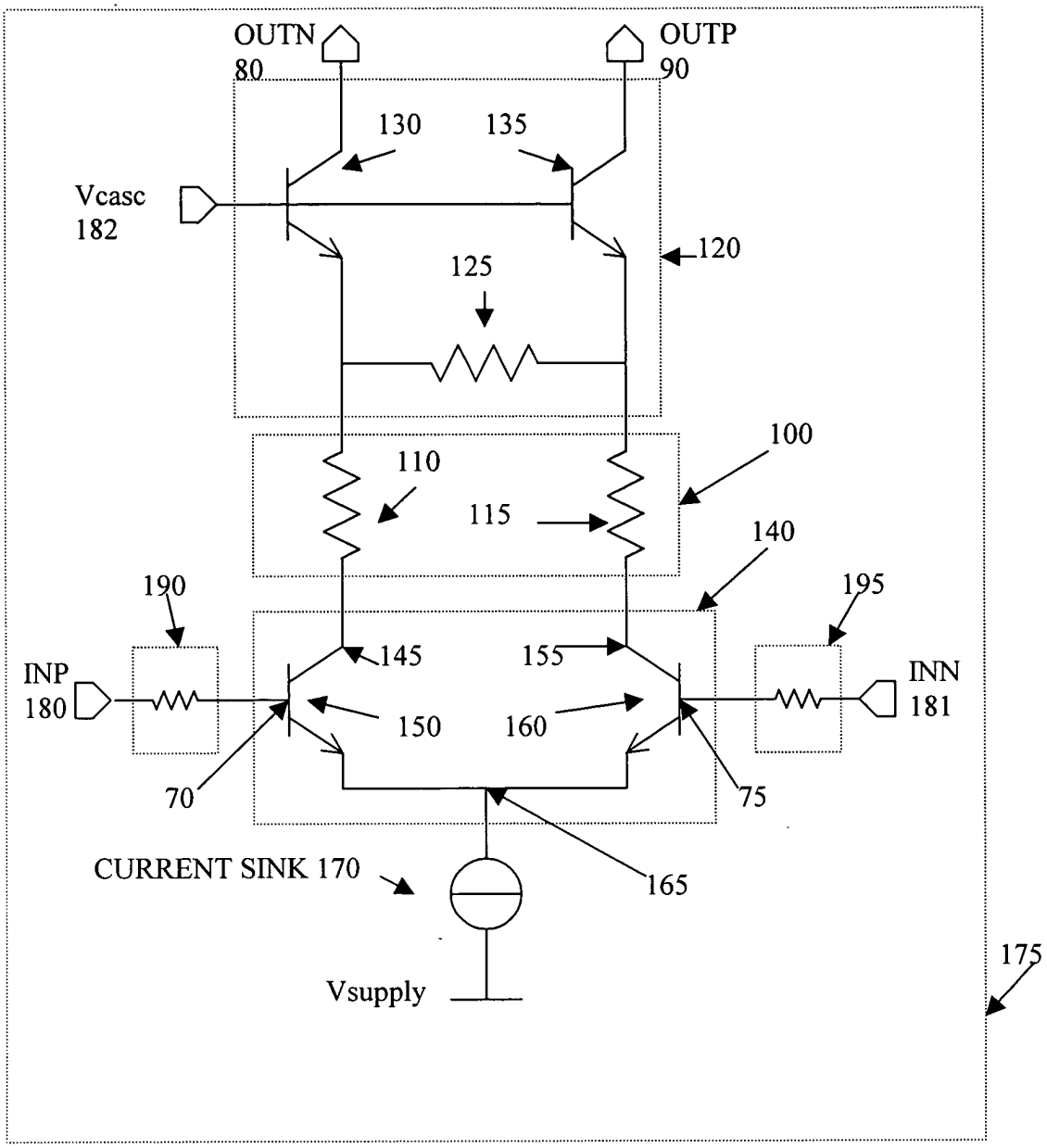
OUTN
80
OUTP
90
130
135
Vcasc
182
120
125
100
110
115
140
190
195
INP
180
145
155
INN
181
150
160
70
75
CURRENT SINK 170
165
Vsupply
175

Figure 1A

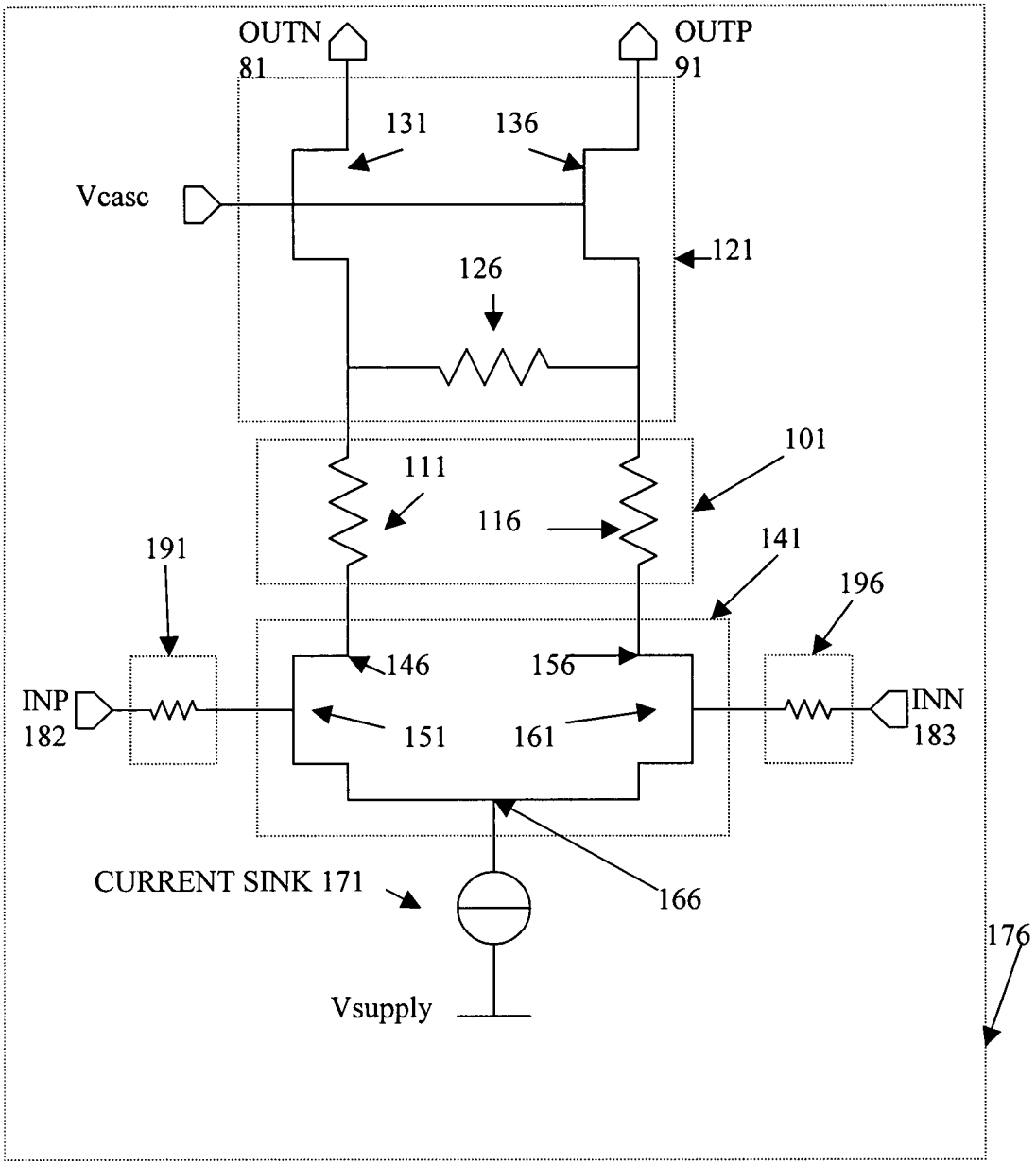
OUTN
81
OUTP
91
131
136
Vcasc
121
126
101
111
116
191
141
196
146
156
INP
182
151
161
INN
183
CURRENT SINK 171
166
176
Vsupply

Figure 1B

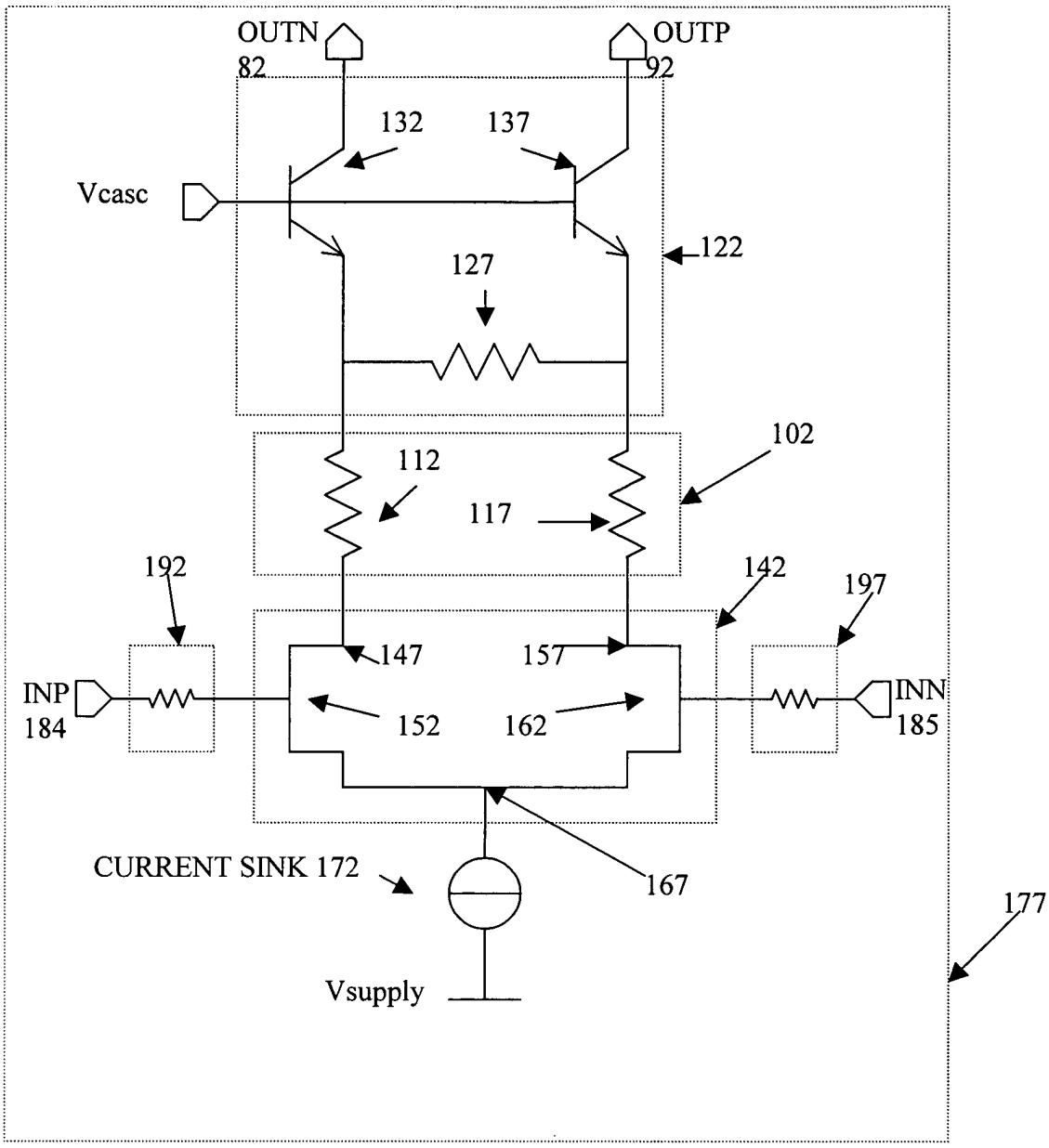
OUTN
82
OUTP
92
132
137
Vcasc
122
127
102
112
117
192
142
197
147
157
INP
184
152
162
INN
185
CURRENT SINK 172
167
177
Vsupply

Figure 1C

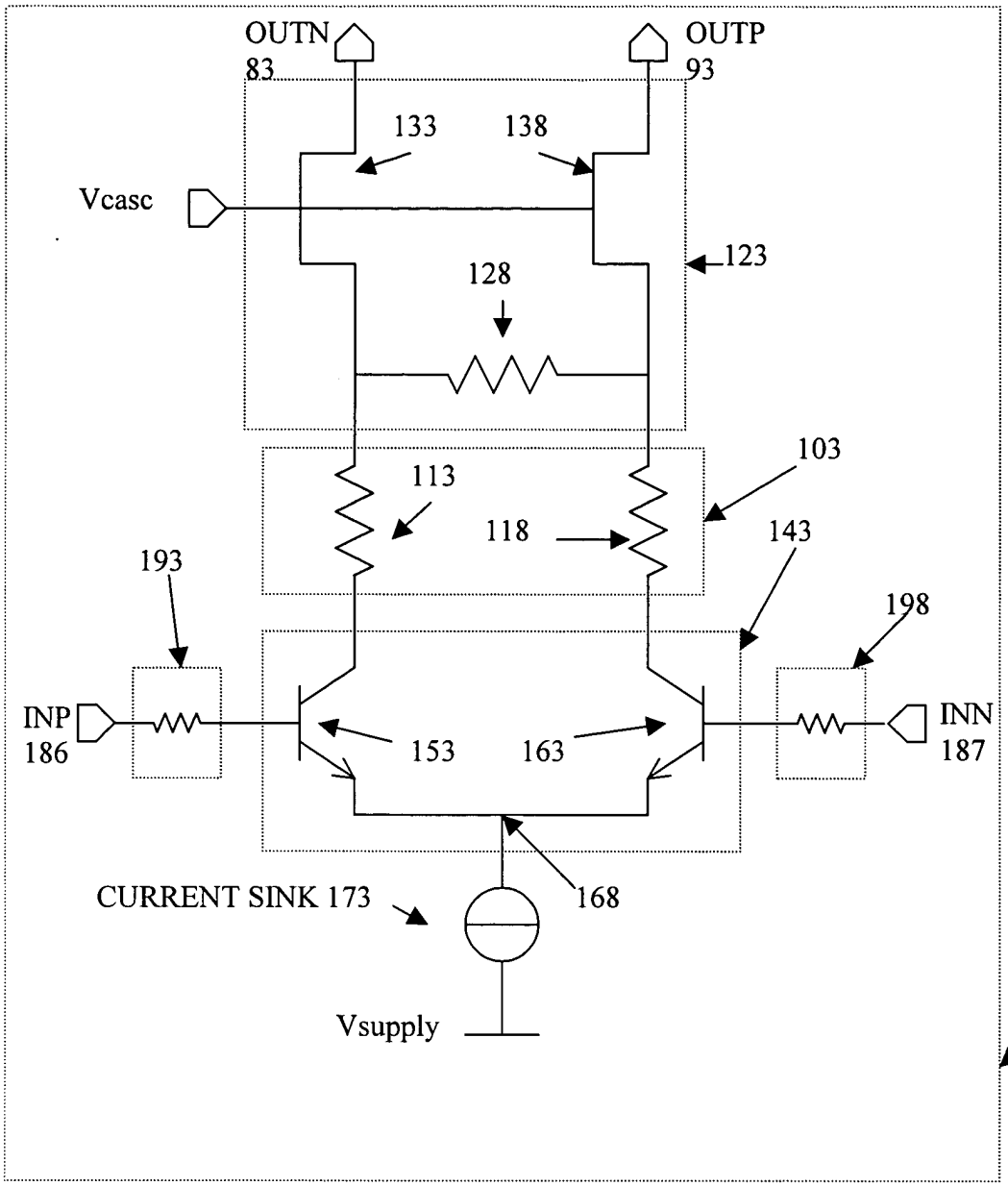
OUTN
83
OUTP
93
133
138
Vcasc
123
128
103
113
118
143
193
198
INP
186
153
163
INN
187
CURRENT SINK 173
168
Vsupply
178

Figure 1D

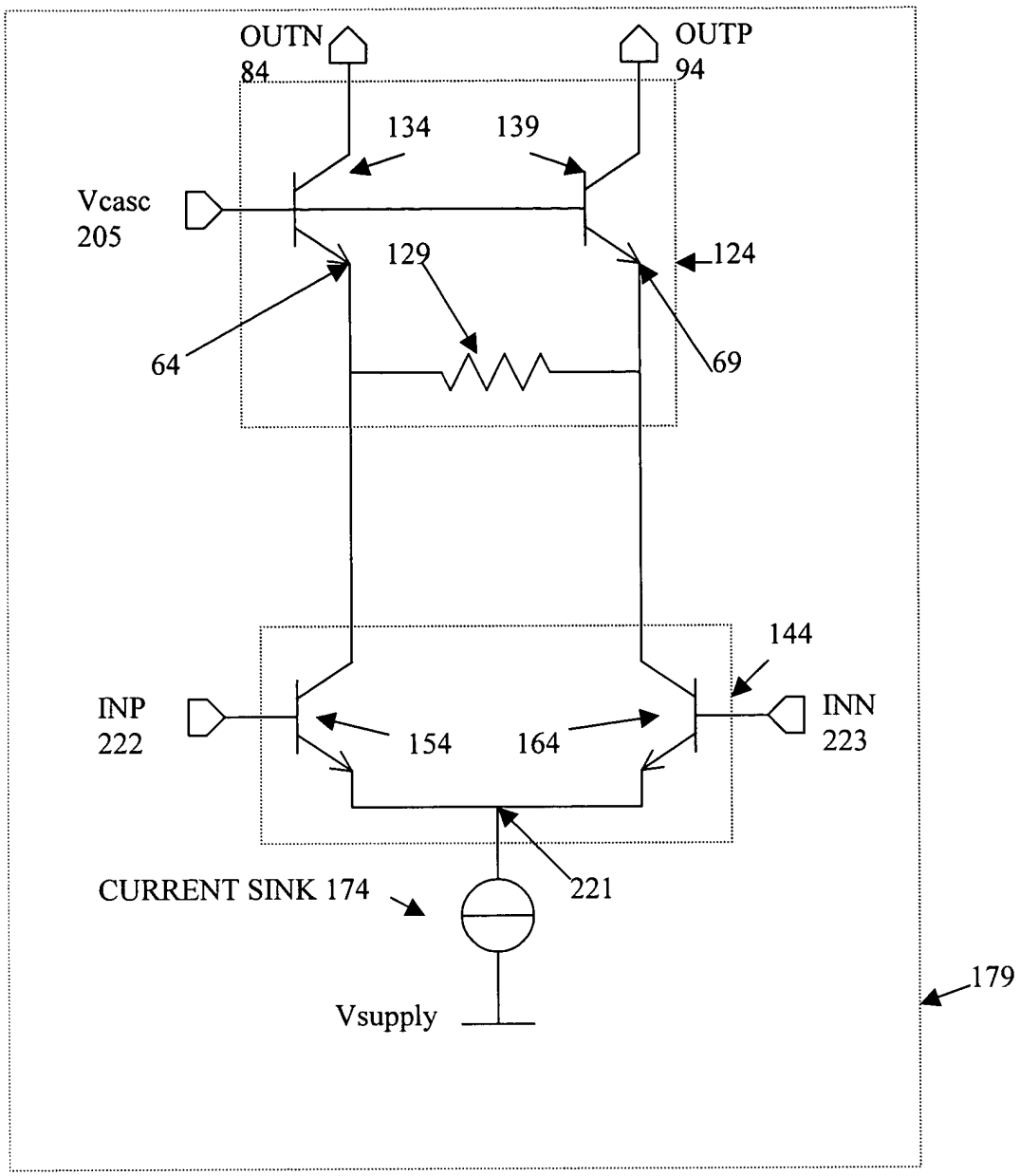
OUTN
84
OUTP
94
134
139
Vcasc
205
129
124
64
69
144
INP
222
154
164
INN
223
CURRENT SINK 174
221
Vsupply
179

Figure 2

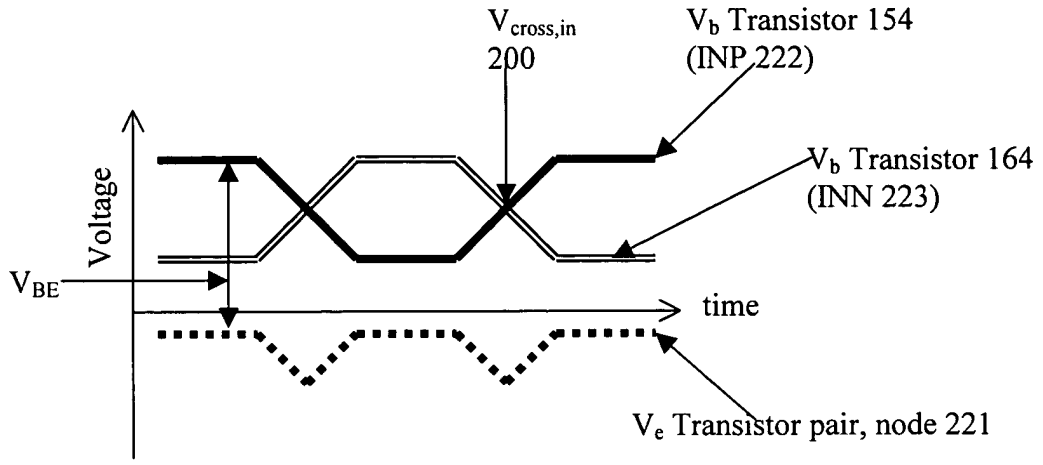
$V_{cross,in}$
200
V_b Transistor 154
(INP 222)
V_b Transistor 164
(INN 223)
Voltage
V_{BE}
time
V_e Transistor pair, node 221

FIG 3a

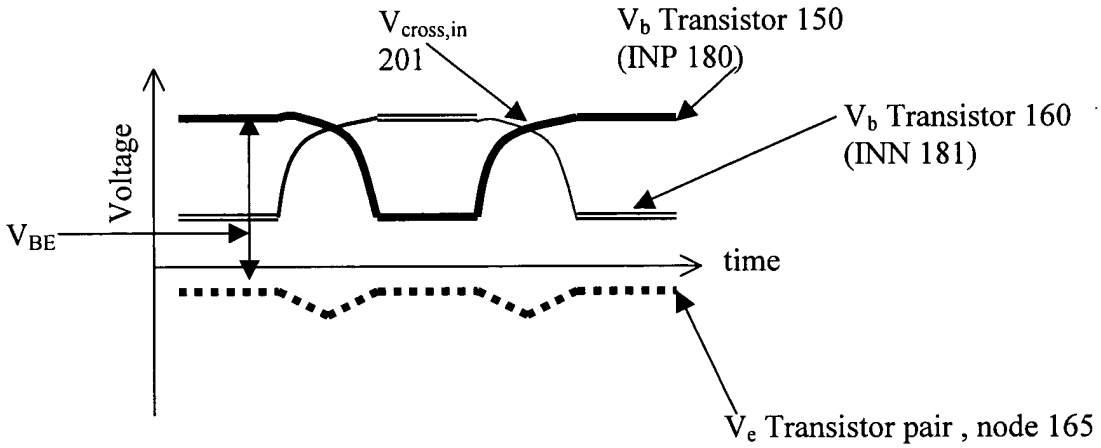
$V_{cross,in}$
201
V_b Transistor 150
(INP 180)
V_b Transistor 160
(INN 181)
Voltage
V_{BE}
time
V_e Transistor pair , node 165

FIG 3b

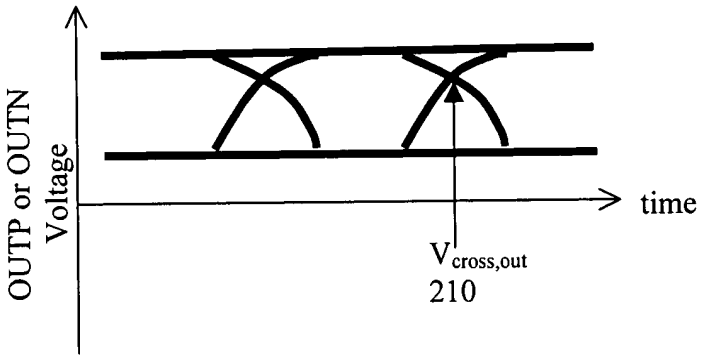
OUTP or OUTN
Voltage
time
$V_{cross,out}$
210

FIG 4a

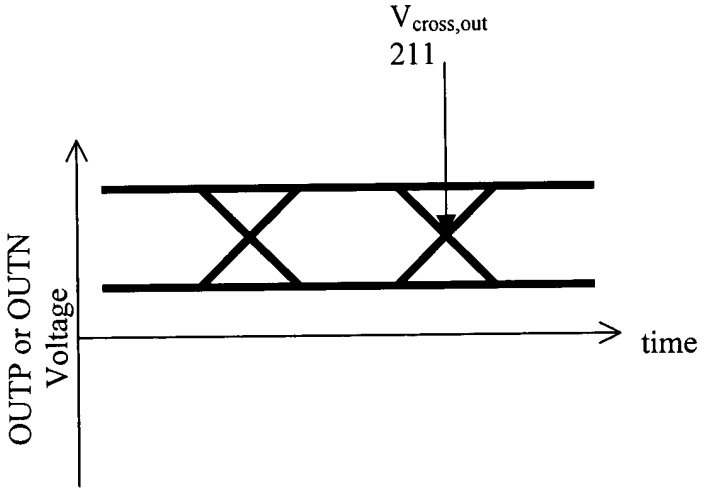
$V_{cross,out}$
211
OUTP or OUTN
Voltage
time

FIG 4b

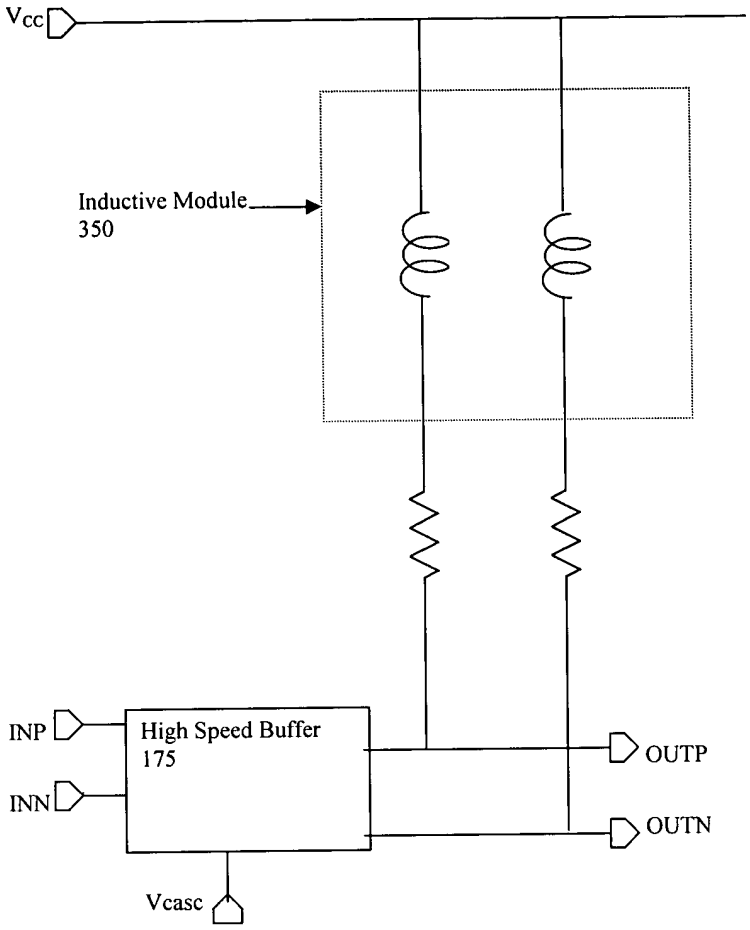
Vcc
Inductive Module
350
INP
INN
High Speed Buffer
175
OUTP
OUTN
Vcasc

Figure 5

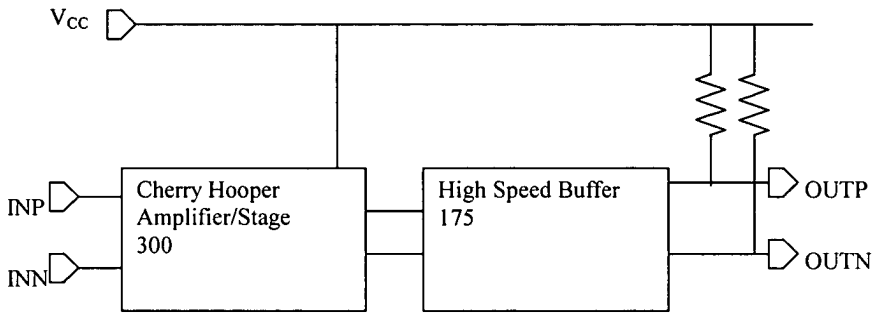
Vcc
INP
INN
Cherry Hooper
Amplifier/Stage
300
High Speed Buffer
175
OUTP
OUTN

Figure 6

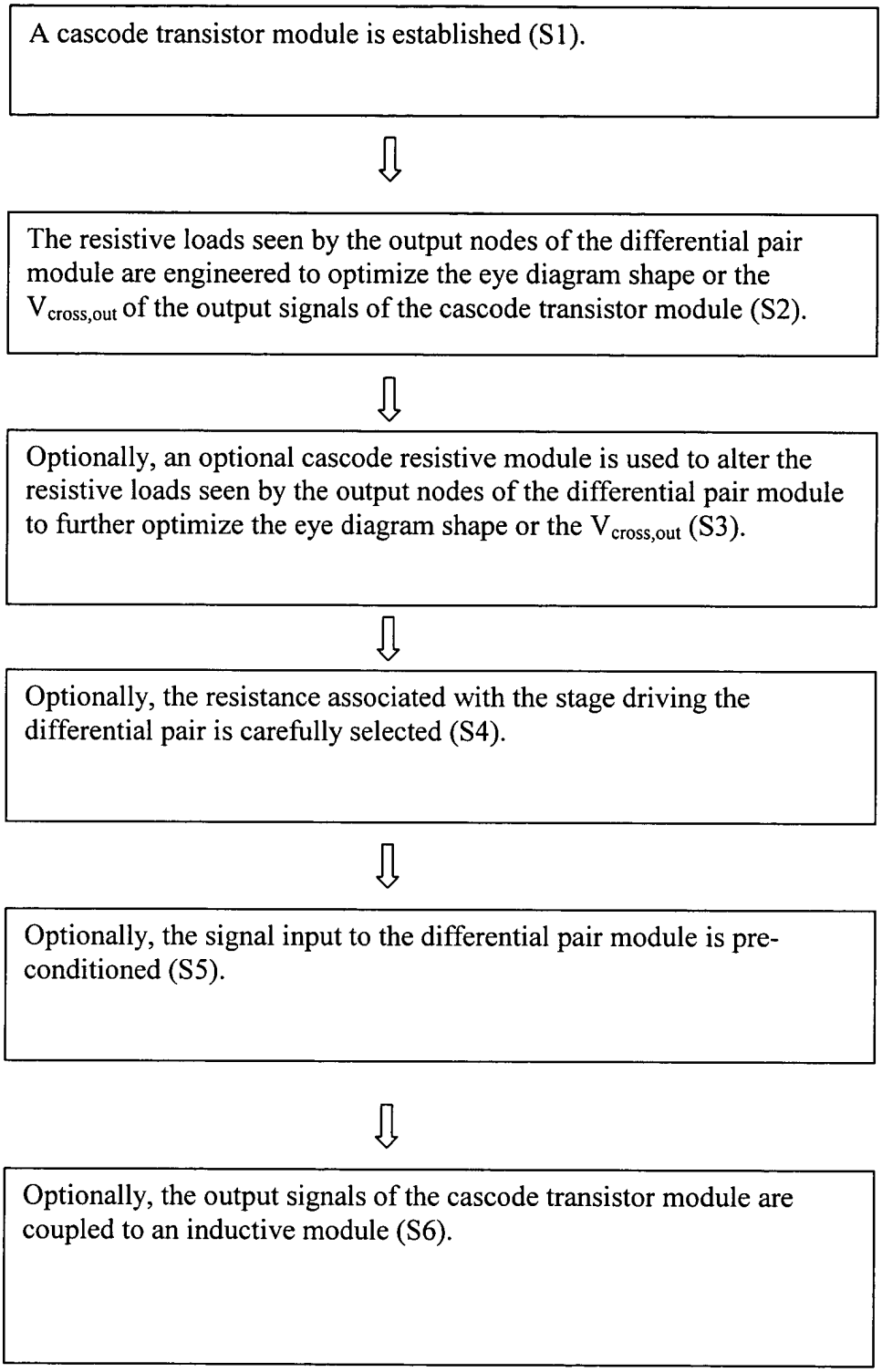
A cascode transistor module is established (S1).
The resistive loads seen by the output nodes of the differential pair module are engineered to optimize the eye diagram shape or the $V_{cross,out}$ of the output signals of the cascode transistor module (S2).
Optionally, an optional cascode resistive module is used to alter the resistive loads seen by the output nodes of the differential pair module to further optimize the eye diagram shape or the $V_{cross,out}$ (S3).
Optionally, the resistance associated with the stage driving the differential pair is carefully selected (S4).
Optionally, the signal input to the differential pair module is pre-conditioned (S5).
Optionally, the output signals of the cascode transistor module are coupled to an inductive module (S6).

Figure 7